REMARKS

The application has been reviewed in light of the Office Action dated June 20, 2006. Claims 1, 2, and 10-16 were pending, with claims 3-9 having previously been canceled (since they were withdrawn by the Patent Office from examination), without prejudice or disclaimer. By this Amendment, new claims 17 and 18 have been added, and claims 1 and 10 have been amended to clarify the claimed invention, without narrowing a scope of the claimed invention. Accordingly, claims 1, 2, and 10-18 are presented for reconsideration, with claims 1 and 10 being in independent form.

Claims 1, 2 and 10-16 were rejected under 35 U.S.C. § 103(a) as purportedly unpatentable over U.S. Patent No. 5,245,215 to Sawaya in view of International Publication No. WO 01/54047 (Sahota et al.).

Applicant has carefully considered the Examiner's comments and the cited art, and respectfully submits that independent claims 1 and 10 are patentable over the cited art, for at least the following reasons.

This application relates to a semiconductor device including plural semiconductor chips integrated into a single package, wherein a first semiconductor chip operates with a first driving voltage at a first level in a digital circuit, and a second semiconductor chip includes circuits which operate with a second level corresponding to a second driving voltage in a digital circuit. As discussed in the background section of the application, the driving voltages of digital devices can vary from one device to another device. Conventionally, a separately packaged voltage level converter device is typically coupled to a digital device which needs to interface with another digital device which operates at a different level than that of the first digital device. In such an arrangement, the system size, cost and complexity of the system (including the first and second

digital devices and the separately packaged voltage level converter device) is relatively high.

Applicant devised an improved semiconductor device including plural semiconductor chips integrated into a single package, wherein a first semiconductor chip operates with and outputs (through a first set of bonding pads) signals at a first level corresponding to a first driving voltage in a digital circuit, and a second semiconductor chip including a signal level conversion circuit which converts the first signals of the first level (received through a second set of bonding pads coupled to the first set of bonding pads) into second signals having a second level different from the first level. Each of independent claims 1 and 10 addresses these features, as well as additional features. In addition, the second semiconductor chip can include digital circuits which are tolerant both to digital input signals of the first level and to digital input signals of the second signal level (claim 17), and/or can receive and operate with signals of the first level as well as signals of a second level corresponding to a second driving voltage in a digital circuit (claim 18).

Sawaya, as understood by Applicant, proposes a multichip packaged semiconductor device having a plurality of LSI chips or discrete semiconductor elements transfer-molded in a single package.

As acknowledged in the Office Action, Sawaya does not teach or suggest, however, a semiconductor device including plural semiconductor chips integrated into a single package, wherein one of the semiconductor chips includes a signal level conversion circuit. Sawaya simply does not disclose or suggest that the multichip packaged semiconductor device proposed therein can be adapted to interface digital circuits operating with one driving voltage and other digital circuits operating with another driving voltage, all within the same integrated package. Sawaya is not directed at the problem that some chips operate at one level while other chips operate at a second level which is different from the first level.

Sahota, as understood by Applicant, proposes a circuit for interfacing digital circuit on the one hand and analog circuits on the other hand. As shown in Fig. 5 of Sahota, the digital circuits 500 and the analog circuits 502 operate with the same driving voltage Vcc.

Applicant does not find disclosure or suggestion in the cited art, however, of a semiconductor device which integrates a plurality of semiconductor chips into a single package, comprising a first semiconductor chip which outputs one or more first signals having a first level, and a second semiconductor chip which includes a signal level conversion circuit, wherein the signal level conversion circuit converts the first signals of the first level from the first semiconductor chip into second signals having a second level different from the first level, and wherein the first level and the second level correspond to respective, different driving voltages in a digital circuit, as provided by the subject matter of claim 1.

Independent claim 10 is patentably distinct from the cited art for at least similar reasons.

Accordingly, for at least the above-stated reasons, Applicant respectfully submits that independent claims 1 and 10, and the claims depending therefrom, are patentable over the cited art.

In view of the amendments to the claims and remarks hereinabove, Applicant submits that the application is now in condition for allowance. Accordingly, Applicant earnestly solicits the allowance of the application.

If a petition for an extension of time is required to make this response timely, this paper should be considered to be such a petition. The Patent Office is hereby authorized to charge any fees that may be required in connection with this amendment and to credit any overpayment to our Deposit Account No. 03-3125.

If a telephone interview could advance the prosecution of this application, the Examiner is

respectfully requested to call the undersigned attorney.

Respectfully submitted,

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